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10/551,571	09/29/2005	Pascal Bolcato	7126-71851-01	4335

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EXAMINER	
LUU, CUONG V	
ART UNIT	**PAPER NUMBER**
2128	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/551,571	BOLCATO ET AL.	
	Examiner	Art Unit	
	Cuong V. Luu	2128	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 September 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *20 September 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *9/29/06, 11/03/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claims 1-20 are pending. Claims 1-20 have been examined. Claims 1-20 have been rejected.

Claim Rejections - 35 USC § 101

35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

Claims 11-16 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter.

1. As per claim 11, it is rejected under 35 U.S.C. 101 because the claimed invention is drawn to program per se. It is trying to claim a simulator comprising a software kernel.

2. Claims 12-16 inherit the defects of claim 11.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-3, 7, 10-13, 16-17, and 20 are rejected under 35 U.S.C. 102(b) as being anticipated by Pino et al (Cosimulating Synchronous DSP Applications with Analog RF Circuits, IEEE 1998, 0-7803-5148-7/98).

1. As per claim 1, Pino teaches method of simulating a circuit, comprising:

reading a description of the circuit that includes a list of components in the circuit and the interconnections between the components, the circuit including both a first set of nodes and components responsive to time-domain signals and a second set of nodes and components responsive to time-frequency domain signals (col. 1 of p. 1710, the Abstract and col. 2 of p. 1710 paragraph 2. Pino's mention of synthesizable DSP transmitter, cosimulating with a RF modulator and power amplifier and EDA tools to perform the cosimulation implies this limitation); and

in a single simulation flow, simulating time-domain representations of signals on the first set of nodes and simulating time-frequency domain representations of signals on the second set of nodes (col. 1 of p. 1710, the Abstract. Pino's teaching of cosimulating of DSP, a time domain representation and RF modulator, a time-frequency domain representation indicates simulating time-domain representations of signals on the first set of nodes and simulating time-frequency domain representations of signals on the second set of nodes in a single flow).

2. As per claim 2, Pino teaches partitioning the circuit into at least one partition including one or more nodes and components from the first set and at least one partition including one or more nodes and components from the second set (col. 2 of p. 1711 section 2.3 Circuit Envelope and fig. 2. Section 2.3 and fig. 2 suggests a portion of circuit including one or more nodes and components from the first set and at least one or more nodes and components from the second set for a hybrid time domain and frequency domain simulation).

3. As per claim 3, Pino teaches the time-domain representations of signals are analog signals included in at least one analog partition and the time-frequency domain representations of signals are RF signals included in at least one RF partition and wherein a solution for simulation of the analog partition affects a solution for simulation of the RF partition (col. 2 of p. 1711 section 2.3 Circuit Envelope and fig. 2).

4. As per claim 7, Pino teaches:

partitioning the circuit into separate modules coupled together, with each module being associated with at least one boundary node external to the module (p. 1713 cols. 1-2 section 4 16 QAM Modem, figures 4-6);

positioning a boundary node by specifying the boundary node to a fixed value (p. 1713 cols. 1-2 section 4 16 QAM Modem, figures 4-6 and col. 2 of p. 1711 section 2.3 Circuit Envelope); and

solving a partitioned module using the fixed value assigned to the positioned boundary node (col. 2 of p. 1711 section 2.3 Circuit Envelope. The simulation of partitioned circuit is solving a partitioned module using the fixed value assigned to the positioned boundary node).

5. As per claim 10, Pino teaches simulating comprises solving analog and RF partitions for each time step H, and wherein the time step H is automatically adjusted based on the simulation results of previous time steps and input stimuli (col. 2 of p. 1711 section 2.3 Circuit Envelope. Pino teaches using SPICE in simulation, which inherits the time step H being automatically adjusted, based on the simulation results of previous time steps and input stimuli).

6. As per claim 11, Pino teaches a simulator for simulating a circuit, comprising:

a single simulator kernel including (col. 1 of p. 1710, the Abstract and col. 2 of p. 1710 paragraph 2):

a) an analog solver simulating a first set of circuit nodes and components using time-domain representations of signals (col. 1 of p. 1710, the Abstract and col. 2 of p. 1710 paragraph 2); and

b) an RF solver simulating a second set of circuit nodes and components using time-frequency domain representations of signals (col. 1 of p. 1710, the Abstract and col. 2 of p. 1710 paragraph 2).

7. As per claim 12, Pino teaches an input to read a net list describing the physical characteristics of the circuit (col. 1 of p. 1710, the Abstract and col. 2 of p. 1710 paragraph 2).

8. As per claim 13, Pino teaches an input to receive control statements from a user to partition the circuit (p. 1713 cols. 1-2 section 4 16 QAM Modem, figures 4-6. Pino teaches partitioning the 16 QAM system into analog RF and DSP. This teaching suggests influence or control statements of the partition by user to an input).

9. As per claim 16, Pino teaches an input to read an analog database and an RF database (col. 1 of p. 1710, the Abstract and col. 2 of p. 1710 paragraph 2).

10. As per claim 17, Pino teaches a system for simulating a circuit, comprising:

means for reading a description of the circuit that comprises a list of components in the circuit and the interconnections between the components, the circuit comprising both a first set of nodes and components responsive to time-domain signals and a second set of nodes and components responsive to time-frequency domain signals (col. 1 of p. 1710 the Abstract and col. 2 of p. 1710 paragraph 2. In these paragraphs Pino teaches using EDA to cosimulate analog and RF circuits; the teaching of using EDA inherits a computer system considered means for in this limitation); and

means for simulating, in a single simulation flow, the first set of nodes using time-domain representations of signals and the second set of nodes using time-frequency domain representations of signals (col. 1 of p. 1710, the Abstract and col. 2 of p. 1710 paragraph 2. In these paragraphs Pino teaches using EDA to cosimulate analog and RF circuits; the teaching of using EDA inherits a computer system considered means for in this limitation).

11. As per claim 20, the discussions in claim 11 inherit the analog solving means and RF solving means within a single simulator kernel.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 4-6, 14-15, and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Pino as applied to claims 1, 11, and 17 above, and further in view of Li et al, hereinafter

Li, (A Frequency Relaxation Approach for Analog/RF System-Level Simulation, ACM 2004, 1-58113-828-8/04/0006).

12. As per claim 4, Pino teaches receiving user input controlling how to partition the circuit (p. 1713 cols. 1-2 section 4 16 QAM Modem, figures 4-6) but does not teach automatically refining the partitions to provide a higher probability of convergence.

    Li teaches this feature (col. 1 of p. 843 the 2nd paragraph).

    It would have been obvious to one of ordinary skill in the art to combine the teachings of Pino and Li. Li's teachings would have facilitated the efficient and accurate analysis of complex response signals over wide frequency ranges (col. 1 of p. 843 the 2nd paragraph).

13. As per claim 5, the discussions in claim 4 suggest partitioning the circuit based on user input and automatically sub-partitioning the circuit to increase simulation speed.

14. As per claim 6, Pino does not teach simulating comprises solving each of the partitions separately and performing relaxations over all of the solved partitions, but Li teaches this limitation (col. 1 of p. 843 2nd paragraph of section 2 Latency in Analog/RF Systems).

    It would have been obvious to one of ordinary skill in the art to combine the teachings of Pino and Li. Li's teachings would quickly have produced a good approximate solution the entire system after several iterations (col. 1 of p. 843 2nd paragraph of section 2 Latency in Analog/RF Systems).

15. As per claim 14, these limitations have already been discussed in claim 4. They are, therefore, rejected for the same reasons.

16. As per claim 15, these limitations have already been discussed in claim 6. They are, therefore, rejected for the same reasons.

17. As per claim 19, these limitations have already been discussed in claim 4. They are, therefore, rejected for the same reasons.

Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Pino as applied to claim 1 above, and further in view of the Applicant's admitted prior art, hereinafter AAPA.

18. As per claim 8, Pino does not teach the time-domain representation of a signal is given by V(t) and the time-frequency domain representation of a signal is given by

$$v(t) = \sum V_k(t)e^{j\omega k^{(t)t}}$$

However, the Applicant's admitted prior art teaches this feature (paragraph 0005).

It would have been obvious to one of ordinary skill in the art to combine the teachings of Pino and the AAPA. The AAPA's teachings would efficiently have handled the modulation information carried by RF signals.

Claims 9 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Pino as applied to claims 1 and 17 above, and further in view of Gabele et al, hereinafter Gabele, (U.S. Pub. 2003/0135354 A1).

19. As per claim 9, Pino does not teach receiving, on a server computer, the description from a client computer over a distributed network, simulating the description on the server computer, and returning results to the client computer over the distributed network.

However, Gabele teaches this limitation (paragraph 0349. In this paragraph Gabele teaches a computer, considered a server, receiving description from another computer, considered a client, to run simulation and then returning the results to the former computer).

It would have been obvious to one of ordinary skill in the art to combine the teachings of Pino and Gabele. Gabele's teachings would have performed simulations of complex and large circuit (paragraph 0008).

20. As per claim 18, these limitations have already been discussed in claim 9. They are, therefore, rejected for the same reasons.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Cuong V. Luu whose telephone number is 571-272-8572. The examiner can normally be reached on Monday-Friday 8:30am-5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kamini Shah, can be reached on 571-272-2279. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300. An inquiry of a general nature or relating to the status of this application should be directed to the TC2100 Group receptionist: 571-272-2100.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

CVL

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